IDT 77211 Errata

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Item Number	Short Description
1	Correction to 128K x 32 SRAM memory map
2	Bus Park is not supported with random (mod 1)
3	Limitation in mixing TSRs with and without interrupt generation
4	Early frame de-assertion on latency timer expiration
5	RxSoc assertion before RxEmpty# deassertion or before RxClav assertion causes incorrect operation

IDT 77211 Errata

Item	Issue	Current Work Around
1	The memory map for the 128K x 32 memory configuration is incorrect in the 77201 User's Manual	TST and SCD memory space is identical to the 32K x 32 memory configuration.

The 128K x 32 memory configuration limits the TST and SCD region to the same space allocated for the 32K x 32 memory configuration. The 128K x 32 memory configuration does allow for additional Rx connections. The memory map for 128K x 32 memory configuration is altered to show as follows:

NICStAR SRAM Memory Map For Using 128k X 32 SRAM

32 Bit Dword Address	Bit 31 ... Bit 0	Byte Address
1 FFFF	**Rx Large Free Buf Queue**	7FFFC
1 FC00	(4K Bytes)	7 F000
1 FBFF	**Rx Small Free Buf Queue**	7 EFFC
1 F800	(4K Bytes)	7 E000
1 F7FF	**Rx Cells FIFO Buffers**	7 DFFC
1 E800	(16K Bytes)	7 A000
1 E7FF	**Variable Rate SCD0**	7 9FFC
1 E7F4	(48 Bytes)	7 9FD0
1 E7F3	**Variable Rate SCD1**	7 9FCC
1 E7E8	(48 Bytes)	7 9FA0
1 E7E7	**Variable Rate SCD2**	7 9F9C
1 E7DC	(48 Bytes)	7 9F70
1 E7DB	**TST and fixed rate SCD region**	7 9F6C
1 C000	(40,816 Bytes)	7 8000
1 BFFF	**Not Used**	6 FFFC
1 0000	(196,608 Bytes)	6 4000
0 FFFF	**Rx Connection Table**	3 FFFC
0 0000	(256K Bytes)	0 0000

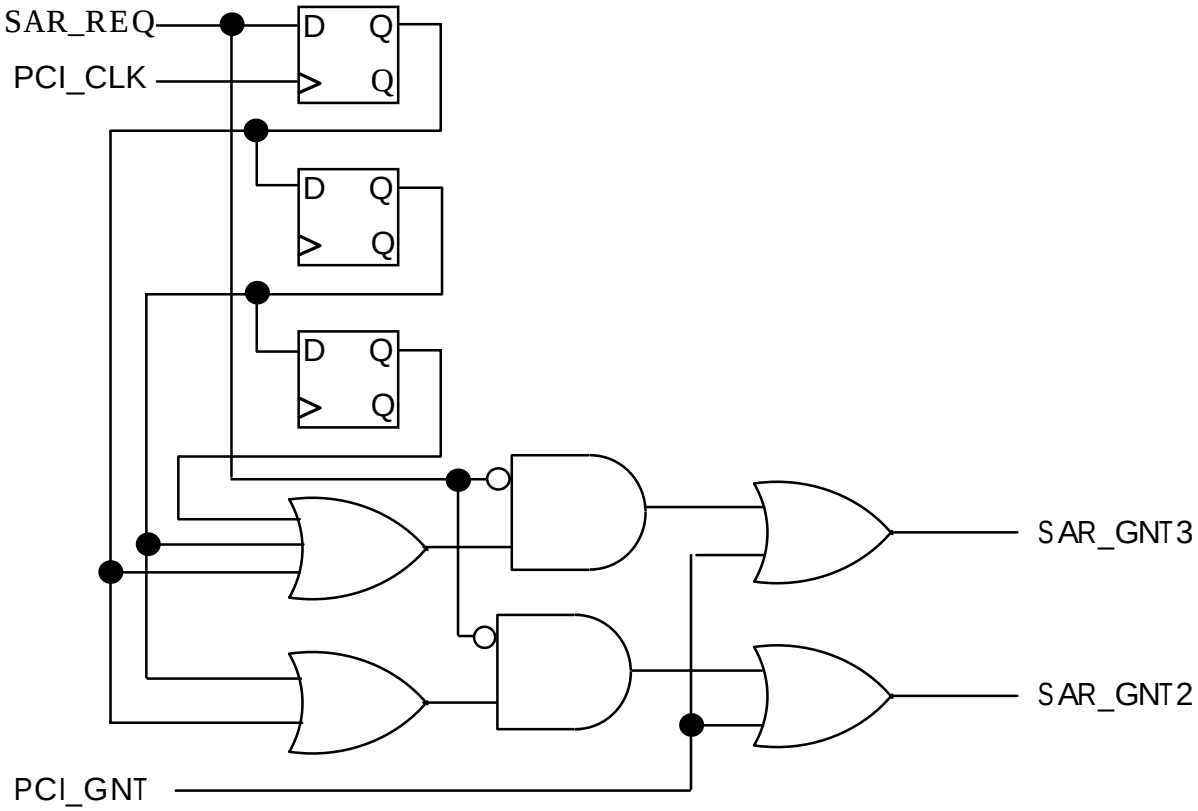
Data drw 50

Note: 32-bit Double word addresses are the SRAM addresses - the byte address is the address written to the command register shifted left by two bits (x4) including the two least significant reserved bits.

Fix: The full address space will be addressable in the 77252 ABR SAR

Item	Issue	Current Work Around
2	Bus Park does not work with random (Mod 1) Tx buffers. This does not effect Mod 48 or Mod 4 Tx buffers.	The addition of one of the PALs defined below.

Bus Park is not supported with random (mod 1) Tx buffers (Mod 4 and Mod 48 are not affected). Delaying the GNT signal two (155Mbps) or three (25Mbps) clocks solves this issue. This can be achieved one of the following PAL configurations:



Layout for 155Mbps and 25Mbps PALs

Item	Issue	Current Work Around
3	Limitation in mixing TSRs with and without interrupt generation	Use only TSRs with interrupts or use only TSRs with out interrupts. ABR version of the SAR will correct this issue.

3. This errata does not affect Tx queues where TSRs always request interrupts or those in which TSRs do not ever request interrupts. The issue arises when a give Tx queue mixes TSRs that require interrupts and TSRs that do not require interrupts. The first TSR requiring an interrupt functions properly. The next TSR that does not request an interrupt will function as though an interrupt was requested. Upon clearing this interrupt, the TSRs function properly until another TSR requesting interrupts is launched and the cycle begins anew.

Fix: Select one of the following:

a. Use only TSRs that request interrupts,
b. Use only TSRs that do not request interrupts,
c. Send a second TSR to clear a TSR interrupt following each TSR requesting interrupts, prior to a TSR not requesting an interrupt.

4	Early frame de-assertion on latency timer expiration	ABR version of the SAR (77252) will correct this issue.

4. When the latency timer expires, the SAR de-asserts FRAME without testing Target Ready. The correct handling would be to hold off de-assertion until Target Ready is asserted.

Fix:

a. ABR SAR (77252) will correct this issue,
b. No conflict has been observed in any commercially available PCI chip set.

5	The 77211 will operate incorrectly if RxSoc is asserted before RxEmpty# is deasserted in byte mode and before RxClav is asserted in cell mode.	Use the AND of RxSoc and RxClav in cell mode and RxSoc and RxEmpty# in byte mode as the new signal input to the 77211's RxSoc pin.

5. If RxSoc is asserted before RxEmpty# is deasserted in byte mode and before RxClav is asserted in cell mode, the 77211 will operate incorrectly.

Example: Picture 3 cycles (byte mode)

Cycle 1: RxSoc asserted, RxEmpty# asserted. (no action)
Cycle 2: RxSoc asserted, RxEmpty# deasserted. (first byte)
Cycle 3: RxSoc deasserted, RxEmpty# deasserted. (second byte)

In the above example the 77211 will interpret the first byte as the second byte and the second byte as the third byte and so on.

Fix:

a. Use the AND of RxSoc and RxClav in cell mode and RxSoc and RxEmpty# in byte mode as the new signal input to the 77211's RxSoc pin.
b. Will be fixed in 77252 ABR SAR.